Materials for Electronics

The U.S. electronics industry faces strong international competition in the manufacture of smaller, faster, more functional, and more reliable products. Many critical challenges facing the industry require the continual development of advanced materials and processes. The NIST Materials Science and Engineering Laboratory (MSEL) works closely with U.S. industry covering a broad spectrum of sectors including semiconductor manufacturing, device components, packaging, data storage, and assembly, as well as complementary and emerging areas such as optoelectronics and organic electronics. MSEL has a multidivisional approach, committed to addressing the most critical materials measurement and standards issues for electronic materials. Our vision is to be the key resource within the Federal Government for materials metrology development and will be realized through the following objectives:

- Develop and deliver standard measurements and data;
- Develop advanced measurement methods needed by industry to address new problems that arise with the development of new materials;
- Develop and apply *in situ* as well as real-time, factory floor measurements, for materials and devices having micrometer- to nanometer-scale dimensions;
- Develop combinatorial material methodologies for the rapid optimization of industrially important electronic materials;
- Provide the fundamental understanding of the divergence of thin film and nanoscale material properties from their bulk values;
- Provide the fundamental understanding of materials needed for future nanoelectronic devices, including first principles modeling of such materials.

The NIST/MSEL program consists of projects led by the Metallurgy, Polymers, Materials Reliability, and Ceramics Divisions. These projects are conducted in collaboration with partners from industrial consortia (*e.g.*, International SEMATECH), individual companies, academia, and other government agencies. The program is strongly coupled with other microelectronics programs within the government such as the National Semiconductor Metrology Program (NSMP). Materials metrology needs are also identified through the International Technology Roadmap for Semiconductors (ITRS), the IPC Lead-free Solder Roadmap, the National Electronics Manufacturing Initiative (NEMI) Roadmap, the Optoelectronics Industry Development Association (OIDA) Roadmap, IPC (the International Packaging Consortium), and the National [Magnetic Data] Storage Industry Consortium (NSIC) Roadmap.

In each of these areas, MSEL researchers have made substantial contributions to the most pressing technical challenges facing industry, from new fabrication methods and advanced materials in the semiconductor industry, to advanced packaging materials, to magnetic data storage. Below are just a few examples of MSEL contributions over the past year.

Advanced Gate Dielectrics

To enable further device scaling, the capacitive equivalent thickness (CET) of the gate stack thickness must be 0.5 nm to 1.0 nm. This is not achievable with existing SiO_2/polcrystalline Si gate stacks. Given the large number of possible choices for these new layers, the only feasible approach to understanding the complex materials interactions that result at the gate dielectric/substrate and gate dielectric/metal gate electrode interfaces is through the application of combinatorial methodologies. This same methodology and apparatus are applicable to a wide variety of problems in the electronic materials field.

Sub-100 nm Nanofabrication

The continual decrease in feature size has been the driving force for advances in the semiconductor industry. Current structures have 90 nm dimensions with planned nodes at 65 nm and 35 nm structures. Advanced measurements of the patterning materials (photoresists), are needed to enable future large scale manufacturing of smaller devices. MSEL utilizes advanced x-ray and neutron tools to provide insight into the feasibility and optimization of these important processes.

Advanced Metallization

Electrodeposited copper is rapidly replacing aluminum for on-chip “wiring” because of its lower electrical resistivity, superior electromigration behavior, and the ability to fill fine features without the formation of seams or voids. As feature dimensions go below 100 nm, difficulties in maintaining performance are anticipated. These issues are addressed through a combination of modeling and experimental efforts.

Test Methods for Embedded Passive Devices

Significant advantages arise if passive devices are integrated directly into the circuit board as embedded passive devices rather than discretely attached with automated assembly. New metrology methods were developed to address the needs of the electronic industry. Two test methods were completed and have received wide acceptance by industry as new methods to accelerate the development of embedded passive device technology.